What Is Claimed Is:

1. An apparatus for routing data between integrated circuit devices, comprising:

an n-dimensional grid of integrated circuit devices;

a plurality of communication networks coupling the n-dimensional grid of integrated circuit devices, wherein a communication network of the plurality of communication networks moves data in only orthogonal dimensions; and

a routing mechanism configured to route data across the plurality of communication networks as well as into, out of, and through a given integrated circuit within the n-dimensional grid of integrated circuits;

whereby a process of routing signals across a given network is greatly simplified because it is not possible to create a cycle that causes a deadlock within the given network; and

whereby the process of routing signals yields a shortest path between source and destination.

2. The apparatus of claim 1, wherein the n-dimensional grid of integrated circuit devices includes memory devices.

3. The apparatus of claim 1, wherein the n-dimensional grid of integrated circuit devices includes processor devices, I/O devices, digital signal processors, field programmable gate arrays, sensors, and controllers.

4. The apparatus of claim 1, wherein the plurality of communication networks for a two-dimensional grid includes:

a first communication network configured to move signals East and North;

a second communication network configured to move signals North and West;

a third communication network configured to move signals West and South;

and

a fourth communication network configured to move signals South and East.

5. The apparatus of claim 1, wherein the routing mechanism is configured to statically route data items across the plurality of communication networks.

6. The apparatus of claim 1, wherein the routing mechanism is configured to dynamically route data items through network junctions within each integrated circuit.

7. The apparatus of claim 1,

wherein a header attached to each data item in a two-dimensional grid indicates a number of horizontal steps and a number of vertical steps required for the data item to reach its destination; and

wherein during a dynamic routing process, the routing mechanism removes a horizontal step or a vertical step from the header for the data item, depending upon which direction is dynamically selected.

8. A method for creating a computing system, comprising:

creating an n-dimensional grid of integrated circuit devices;

establishing a plurality of communication networks coupling the n-dimensional grid of integrated circuit devices, wherein a communication network of the plurality of communication networks moves data in only orthogonal dimensions; and

providing a routing mechanism configured to route data across the plurality of communication networks as well as into, out of, and through a given integrated circuit within the n-dimensional grid of integrated circuits;

whereby a process of routing signals across a given network is greatly simplified because it is not possible to create a cycle that causes a deadlock within the given network; and

whereby the process of routing signals yields a shortest path between source and destination.

9. The method of claim 8, wherein the n-dimensional grid of integrated circuit devices includes memory devices.

10. The method of claim 8, wherein the n-dimensional grid of integrated circuit devices includes processor devices, I/O devices, digital signal processors, field programmable gate arrays, sensors, and controllers.

11. The method of claim 8, wherein the plurality of communication networks for a two-dimensional grid includes:

a first communication network configured to move signals East and North;

a second communication network configured to move signals North and West;

a third communication network configured to move signals West and South;

and

a fourth communication network configured to move signals South and East.

12. The method of claim 8, wherein the routing mechanism is configured to statically route data items across the plurality of communication networks.

13. The method of claim 8, wherein the routing mechanism is configured to dynamically route data items through network junctions within each integrated circuit.

14. The method of claim 8,

wherein a header attached to each data item in a two-dimensional grid indicates a number of horizontal steps and a number of vertical steps required for the data item to reach its destination; and

wherein during a dynamic routing process, the routing mechanism removes a horizontal step or a vertical step from the header for the data item, depending upon which direction is dynamically selected.

15. A means for routing data between integrated circuit devices within an n-dimensional grid of integrated circuit devices, comprising:

a communication means comprising a plurality of communication networks coupling the n-dimensional grid of integrated circuit devices, wherein a communication network of the plurality of communication networks moves data in only orthogonal dimensions; and

a routing means for routing data across the plurality of communication networks as well as into, out of, and through a given integrated circuit within the n-dimensional grid of integrated circuits;

whereby the means of routing signals yields a shortest path between source and destination.

16. The means of claim 15, wherein the n-dimensional grid of integrated circuit devices includes memory devices.

17. The means of claim 15, wherein the n-dimensional grid of integrated circuit devices includes processor devices, I/O devices, digital signal processors, field programmable gate arrays, sensors, and controllers.

18. The means of claim 15, wherein the plurality of communication networks for a two-dimensional grid includes:

a first communication network configured to move signals East and North;

a second communication network configured to move signals North and West;

a third communication network configured to move signals West and South;

and

a fourth communication network configured to move signals South and East.

19. The means of claim 15, wherein data is configured to statically routed across the plurality of communication networks.

20. The means of claim 15, wherein data is dynamically routed through network junctions within each integrated circuit.

21. The means of claim 15,

wherein a header attached to each data item in a two-dimensional grid indicates a number of horizontal steps and a number of vertical steps required for the data item to reach its destination; and

wherein during a dynamic routing process, a horizontal step or a vertical step is removed from the header for the data item, depending upon which direction is dynamically selected.